A Nonlinear GaAs FET Model for Use in the Design of Output Circuits for Power Amplifiers

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Abstract—**A nonlinear equivalent circuit model for the GaAs FET has been developed based upon the small-signal device model and separate current measurements, including drain-gate avalanche current data. The harmonic-balance technique is used to develop the FET RF load-pull characteristics in an amplifier configuration under large-signal operation. Computed and experimental load-pull results show good agreement.**

I. Introduction

THE GENERAL-PURPOSE nonlinear circuit analysis programs that exist were designed primarily for transient (time-domain) analysis of silicon integrated circuits [1], [2]. By adding new models for GaAs devices, Curtice [3] and Sussman-Fort *et al.* [4] show that these programs can be used for the study of GaAs integrated circuits. However, a more sophisticated model is required to study GaAs power FET's operated at high dc-to-RF conversion efficiency. Such a model must contain an accurate description of all important device nonlinearities and also efficiently analyze the external microwave circuit interaction over many RF cycles. The circuit reactances lead to time constants large relative to the RF period. Time-domain analysis is thus inefficient and, in fact, unnecessary since the reactances are linear.

Rizzoli *et al.* [5] described a general-purpose nonlinear microwave circuit design technique that efficiently analyzes the device–circuit interaction by application of the "harmonic-balance" technique [6]. Camacho-Penalosa [7] described the application of this technique to the microwave FET.

In GaAs power amplifiers, the load-pull method is often used to experimentally obtain optimum load conditions at large-signal operation [8]. Sechi [9] developed a graphical extension of this technique to maximize the RF power output subject to a specified maximum value of intermodulation distortion. However, the load-pull measurements are time consuming and difficult at high RF frequencies. An analytical technique would be very advantageous.

Tajima and Miller [10], Willing *et al.* [11], Peterson *et al.* [12], and others have reported nonlinear GaAs FET models for the design of power amplifiers. We have extended the work of Peterson *et al.* and made detailed comparisons of computed and measured load-pull characteristics using a nonlinear analysis program for the GaAs FET amplifier based upon the harmonic-balance technique.

Materka and Kacprzak [13] recently proposed a large-signal analysis of a GaAs FET amplifier. Our model is similar but has significant differences in detail. We measure avalanche breakdown voltage for devices and use these values in the analytical model. The nonlinear gate-to-source capacitance variation that we measure is different from the ideal variation assumed by Materka and Kacprzak. We also include second- and third-harmonic voltages in the analysis and show this to be significant. Nevertheless, the agreement shown by Materka and Kacpzak between their measurements and model calculations is excellent.

Our nonlinear device model has evolved from the self-consistent GaAs FET small-signal model reported by Curtice and Camisa [14]. This program provides a computer-aided means to develop output circuit designs that optimize the amplifier performance (i.e., efficiency, bandwidth, etc.). Accurate prediction of large-signal load-pull performance is essential to accurately design output networks. In addition, we operate the program on Hewlett-Packard 1000 RTE minicomputers to reduce the cost of computation.

Section II reviews the nonlinear analysis program. The FET model and the method of evaluation of the nonlinearities are presented in Section III. Mathematical equations are presented in Section IV. The remaining sections describe analytically generated load-pull results and their comparison with measured load-pull data. Large-signal FET simulations by the nonlinear program are also compared with simulations from a two-dimensional device model. This comparison shows the importance of including the third harmonic of voltage in the output circuit.

II. The Nonlinear FET Program

This program consists of a time-domain model of the GaAs MESFET coupled with frequency-domain models for the input and output matching circuits. The nonlinear FET elements must be analyzed in the time domain to preserve their physical nature. The linear circuit response to the FET current excitation can be analyzed in the frequency domain by standard techniques. Transformation

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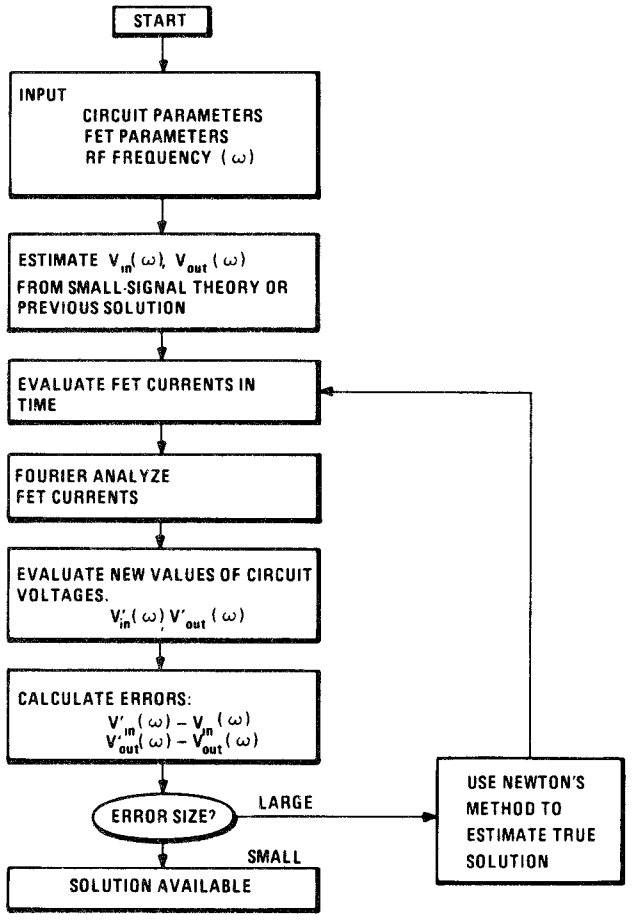


Fig. 1. Program flow chart.

between the time and the frequency domains is accomplished using a discrete Fourier transform. A valid physical solution is obtained when the voltage waveform at the input (or output) of the FET produces a current waveform into the device that is the negative of that into the RF circuit to within some small error. The program flow chart is shown in Fig. 1. The method of successive approximation is used with less than 100-percent update to assure convergence.

III. Evaluation GaAs MESFET Nonlinearities

Fig. 2 shows the equivalent circuit model assumed. This model is noticeably different than used by Curtice and Camisa for accurate small-signal modeling of GaAs MESFET's. The drain-channel capacitor is omitted to simplify node current equations. This produces some loss of accuracy. In addition, two new current sources are used. The drain-gate voltage-controlled current source represents the drain-gate avalanche current that can occur at large-signal operation. The gate-source voltage-controlled current source represents gate current that occurs when the gate-source junction is forward biased. The third current source $I_{ds}(V_{in}, V_{out})$ is the large-signal form of the usual small-signal transconductance.

Fig. 3 shows the measured dc current-voltage relationship for an RCA device studied. This data is measured in the automated Fukui [15] equipment, and Kelvin probes are used (and required) to obtain accurate data. Fig. 4 shows data on the same device for larger drain-source voltages. The data for higher currents in Fig. 3 are appreciably influenced by heating effects. However, this should not cause large error in the nonlinear model. Fig.. 4 shows that the device pinchoff voltage increases appreciably at larger drain-source voltage. The early version of the nonlinear program assumed a square-law relationship between the (saturation) current and the gate-source voltage. Real devices often do not exhibit such a relationship and it is more accurate to use a cubic approximation

$$I_{ds} = \left(A_0 + A_1 V_1 + A_2 V_1^2 + A_3 V_1^3\right) \cdot \tanh\left(\gamma \cdot V_{out}(t)\right)$$

where V_1 is the input voltage. The coefficients A_i can be evaluated from data in the saturation region at the same time the data of Fig. 12 is measured. We use a simple Fortran program for evaluation of the A_i's with least-square error. One disadvantage of the cubic relationship is that unlike the quadradic, a pinchoff voltage may result that makes current zero or transconductance zero, but not both.

The following method is used to include the phenomenon of pinchoff voltage increase with drain-source voltage (Fig. 4). We assume

$$V_1 = V_{in}(t - \tau) \cdot \left[1 + \beta\left(V_{out}^0 - V_{out}(t)\right)\right]$$

where

β coefficient for pinchoff change,
V_{out}^0 output voltage at which A_0, A_1, A_2, A_3 were evaluated, and
τ internal time delay of FET.

The form of this equation is not physically significant. Measured RF data (see Appendix A) shows that τ is a direct function of drain-source voltage, or

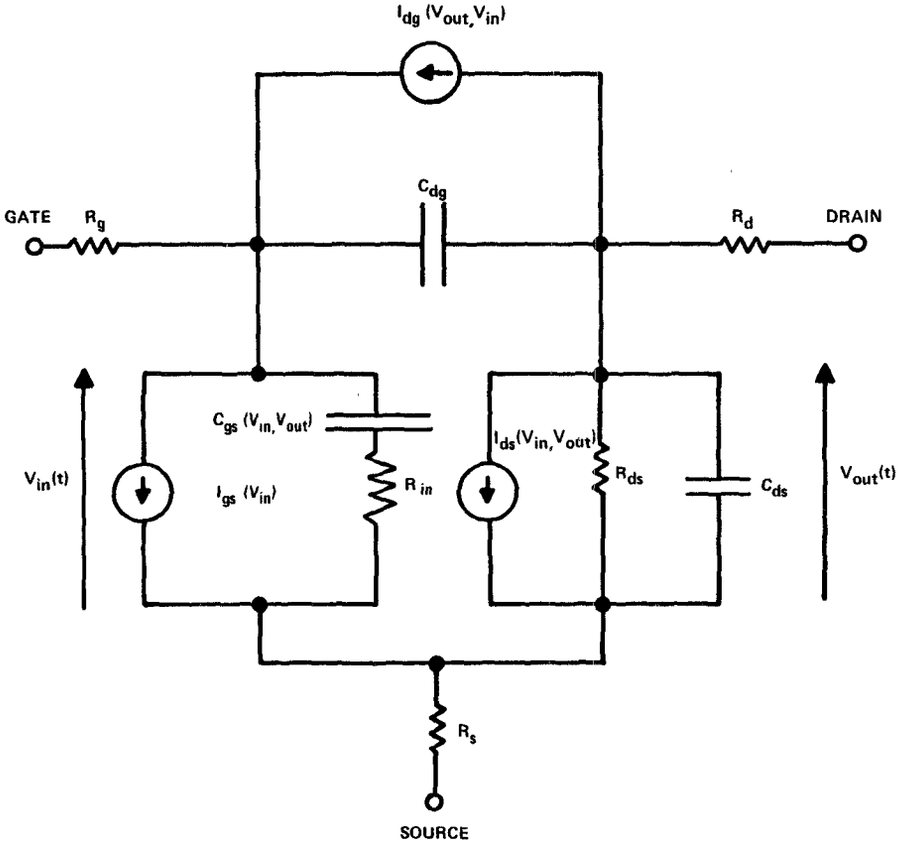
$$\tau = A_5 \cdot V_{out}(t).$$

Fig. 5 shows the current-voltage relationship calculated using these equations for the RCA device whose characteristics were shown in Figs. 3 and 4. This technique produces an accurate approximation to the measured data.

Pulsed measurement of drain-gate avalanche currents were made on a number of devices. Fig. 6 shows data for the device previously studied (Figs. 3 and 4). Notice that the drain currents cannot be pinched off at large drain-source voltages due to the gate current produced by avalanche breakdown. This is an important phenomenon that limits both RF current and power output. In this model, the drain-gate avalanche current is taken to be

$$I_{dg} = \begin{cases} \dfrac{V_{dg}(t) - V_B}{R_1}, & V_{dg} > V_B \\ 0, & V_{dg} < V_B \end{cases}$$

where $V_B = V_{B0} + R_2 \cdot I_{ds}$, R_1 is the approximate breakdown resistance, and R_2 is the resistance relating breakdown voltage to channel currents.



EQUIVALENT CIRCUIT OF GaAs MESFET

Fig. 2. Equivalent circuit model of the GaAs MESFET.

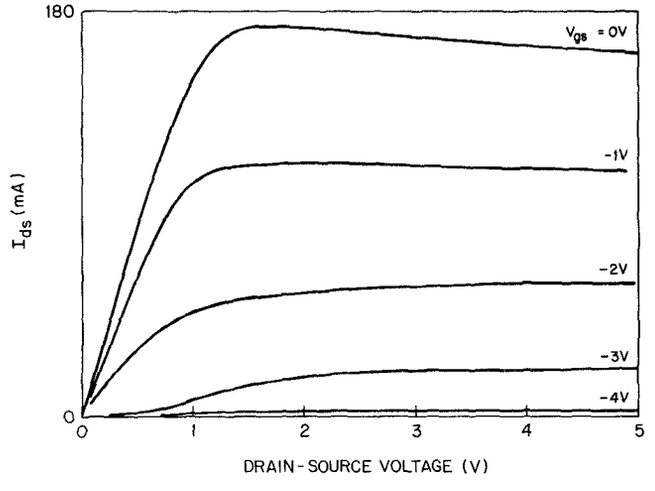


Fig. 3. Measured current–voltage relationship for RCA device B1512-3A.

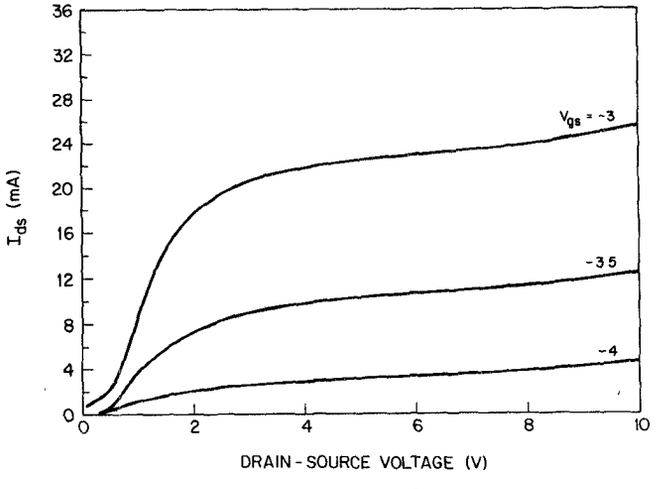


Fig. 4. Same as Fig. 12 but for larger drain-source voltages.

The forward-biased gate current is taken to be

$$I_{gs} = \begin{cases} \dfrac{V_{in}(t) - V_{bi}}{R_F}, & V_{in}(t) \geq V_{bi} \\ 0, & V_{in}(t) < V_{bi} \end{cases}$$

where V_{bi} is the built-in voltage and R_F is the effective value of forward-bias resistance.

The values of R_g, R_d, and R_s are obtained from the automated Fukui measurements. The values of C_{dg}, C_{gs}, R_{ds}, and C_{ds} at the bias point are obtained from the small-signal model using the technique developed by Curtice and Camisa. Although both C_{gs} and C_{dg} are nonlinear functions of voltage, computation including these characteristics produced only small effects upon the RF saturation characteristics.

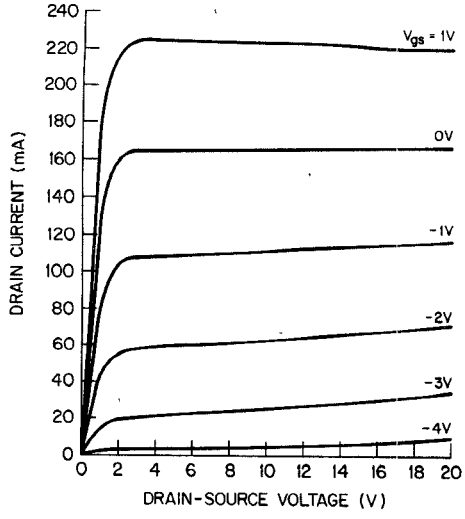


Fig. 5. Current–voltage relationships for RCA device B1512-3A as calculated by the analytical equations.

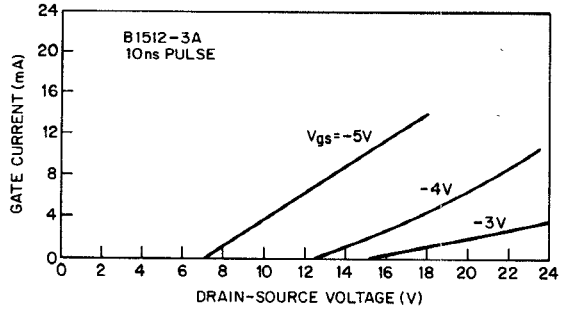


Fig. 6. Pulsed current–voltage data for RCA device B1512-3A.

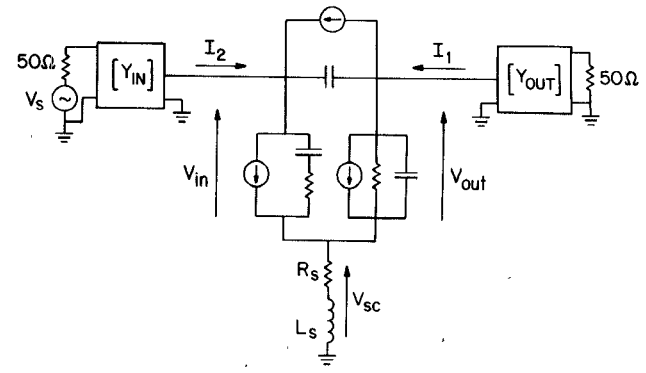


Fig. 7. Equivalent circuit model of GaAs MESFET amplifier as used in the nonlinear analysis program.

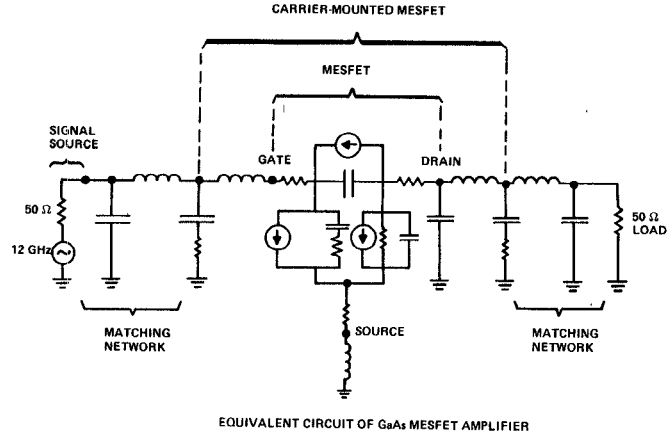


Fig. 8. Equivalent circuit model of GaAs MESFET amplifier showing specific topology for matching circuits.

The drain-source resistance is also a strong function of V_{gs} and V_{ds}. However, differentiation of the drain current in the model gives the following result for small-signal output RF conductance:

$$g_{ds} = \frac{1}{R_{ds}} - g_{m0}\beta V_{\text{in}} + \frac{\gamma I_{ds} \cdot \operatorname{sech}^2[\gamma V_{\text{out}}(t)]}{\tanh(\gamma V_{\text{out}}(t))}$$

where

$$g_{m0} = (A_1 + 2A_2V_1 + 3A_3V_1^2) \cdot \tanh[\gamma \cdot V_{\text{out}}(t)].$$

The three terms comprising g_{ds} may be understood to be: 1) a fixed conductance term; 2) a substrate conductance term that causes the pinchoff voltage change with V_{ds}; and 3) a channel conductance term that is important only at low drain-source voltages (i.e., below current saturation). The net result is that the output RF conductance depends upon V_{gs} and V_{ds} consistent with actual device behavior.

The small-signal intrinsic transconductance can similarly be evaluated by differentiation of drain current with respect to V_{in}. The result is

$$g_m = g_{m0}[1 + \beta(V_{\text{out}}^0 - V_{\text{out}}(t))].$$

Coefficient β causes the transconductance to decrease with increasing drain-source voltage, consistent with the behavior of GaAs FET's.

In summary, the equivalent circuit model has been constructed with the simplified circuit shown in Fig. 2. The principal nonlinearities are the voltage-controlled current sources. These must be characterized for each device. It was found to be important to include the bias dependance of pinchoff voltage in the drain-current source. The small-signal properties of the model were found to be consistent with the FET behavior.

IV. Description of the Computer Program NFET

The program NFET was described briefly in Section II. We now describe the analysis of the FET amplifier using this program.

Fig. 7 shows the lumped-element equivalent circuit model of the GaAs MESFET amplifier. The two-port networks $[Y_{\text{in}}]$ and $[Y_{\text{out}}]$ are matching networks presumably designed for maximum power transfer at the input and the output, respectively. Notice that the gate and drain resistances of the FET are absorbed into these networks. Fig. 8 shows a typical topology for a carrier-mounted FET. The first design of these networks is usually done using SUPER-COMPACT™ [16] to achieve conjugate matching at input and output for small-signal operation. This produces the maximum gain condition. Once a trial design is available, the Y-transfer characteristics can be evaluated.

The input voltage is

$$V_{\text{in}}(t)+V_{sc}(t)=V_{gs}^{dc}+\sum_n\left[a_n\sin(n\omega t)+b_n\cos(n\omega t)\right]$$

where $V_{sc}(t)$ is the voltage drop across the source resistance and inductance which is assumed to be

$$V_{sc}(t)=V_{sc}^{dc}+\sum_n\left[c_n\sin(n\omega t)+d_n\cos(n\omega t)\right].$$

The output device voltage is

$$V_{\text{out}}(t)+V_{sc}(t)=V_{ds}^{dc}+\sum_n\left[f_n\sin(n\omega t)+g_n\cos(n\omega t)\right].$$

The present version of NFET uses dc, fundamental-, second-, and third-harmonic voltage components. The time-domain expressions for $V_{\text{in}}(t)$ and $V_{\text{out}}(t)$ are used to generate device currents. For example, the total drain current consists of drain-source current

$$I_{ds}\left[V_{\text{in}}(t),V_{\text{out}}(t)\right]+C_{ds}\frac{d}{dt}V_{\text{out}}(t)+\frac{V_{\text{out}}(t)-V_{\text{out}}^{dc}}{R_{ds}}$$

plus drain-gate displacement current

$$C_{dg}\frac{d}{dt}\left[V_{\text{out}}(t)-V_{\text{in}}(t)\right]$$

and the avalanche current if $[V_{\text{out}}(t)-V_{\text{in}}(t)]>$ the breakdown voltage V_B.

The drain and gate currents are then Fourier analyzed to find their frequency components using a discrete Fourier transform. Linear circuit elements, such as C_{dg}, need not be included since the answers are known *a priori*.

V. FET Load-Pull Simulation

As an application of the nonlinear analysis program (NFET), a load-pull program was written to simulate the FET performance at high drive levels under variable load conditions. The program runs interactively on the HP1000/A900 and plots contours of constant power output on a Smith Chart.

The algorithm which controls the load pull relies on the fact that the contours of constant power are closed curves and that the power within a given contour is higher than the contour power while the power outside is lower than the contour power. The load pull is designed to proceed in a counterclockwise direction from the first point designated as a contour point. A test point is taken by increasing the radius vector of the reflection coefficient to the given point. If the power at the test point is greater than the contour power, the test point rotates clockwise to find the next contour point. If the test point gives a lower power, then it is outside the contour and the test point is rotated counterclockwise to find the next contour point. The "width" of the contour is programmable and is usually taken as 1 percent of the contour power. If the calculated power points fall outside this limit, the algorithm interpolates between the two nearest values.

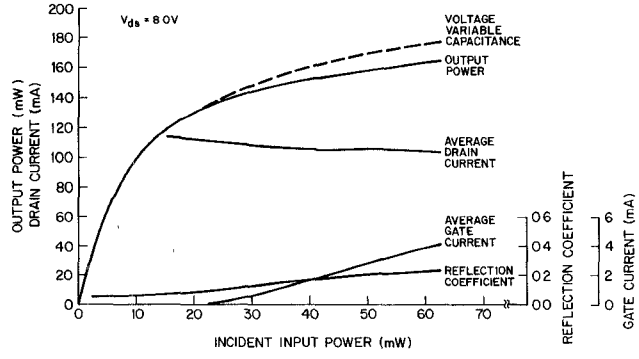


Fig. 9. Output RF power, average drain current, average gate current, and reflection coefficient as a function of RF input power for RCA device B1512-3A at 12 GHz with $V_{ds}=8$ V, $V_{gs}=-1$ V. The output is tuned for high gain.

VI. Comparison with Experimental Data

Fundamental- and second-harmonic voltages are used for the calculation presented in this section. Fig. 9 shows the calculated RF power output as a function of RF power input for RCA device B1512-3A for a case of output matching for high gain. Strong output power saturation occurs due to the large RF voltage amplitudes. As the degree of saturation increases with increase of RF input power, the computed average drain current decreases, the average gate current increases, and the reflection coefficient at the input increases as seen in Fig. 9. These effects are in agreement with experimental observations. These calculations were made assuming a constant value of gate-source capacitance. The dashed output power curve shows the result for voltage-variable gate-source capacitance. Here a square-root relationship was assumed with a built-in voltage of 1 V. This variation is much larger than measured but produces less than a 10-percent increase in the output power. Therefore, the assumption of a constant gate-source capacitance does not greatly effect the accuracy of the results. The reason for this behavior is described in Appendix B.

By reducing the shunt resistive loading of the output circuit, higher RF power output can be achieved. Fig. 10 shows the input/output power relationship calculated at two different output loadings. The case of lower shunt impedance (73 Ω) is very similar to the measured data (also plotted in Fig. 10). However, there is more gain and more (forward-biased) gate current in the calculated results. This indicates that the model does not fully reproduce the operating conditions.

The power data of Fig. 10 are replotted in Fig. 11 using a logarithmic scale. Note that there is about 2-dB difference in the power gain for the data and the lower shunt impedance case. A portion of the 2 dB is believed to be due to input losses in the tuner used in the measurements.

Load-pull contours are developed as follows: The load is adjusted for maximum output power for a given RF drive power. Then the load is changed to produce less output power (e.g., −1 dB), and a load contour for constant power is measured.

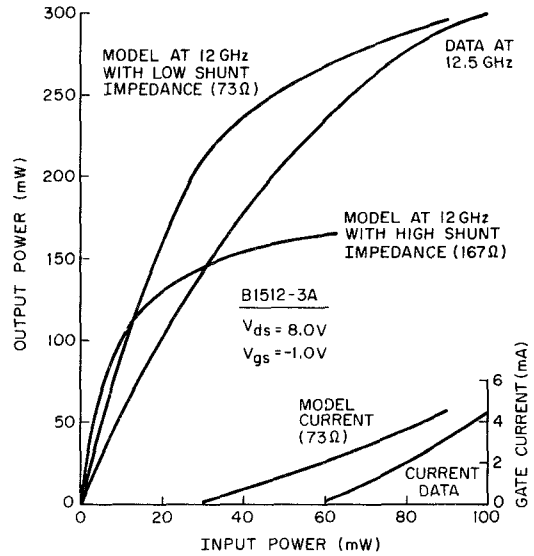


Fig. 10. RF power output as a function of RF power input for device B1512-3A with $V_{ds} = 8$ V, $V_{gs} = -1$ V. The curves starting at origin are calculated at 12 GHz and the third curve is measured data at 12.5 GHz.

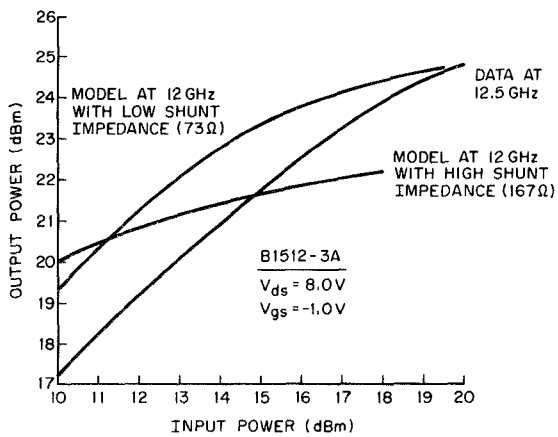


Fig. 11. Measured and calculated RF power output as a function of RF power input for device B1512-3A with $V_{ds} = 8$ V, $V_{gs} = -1$ V, and plotted on a logarithmic scale.

Fig. 12 shows the calculated and measured load-pull contours (for a nominal maximum output power of 200 mW) for this device for 176- and 145-mW power output at 12 GHz. The agreement is good. Fig. 13 shows the calculated and measured points of the load for maximum power output for various output power values. These do not agree as well as seen in other devices.

Fig. 14 shows the effect of harmonic voltages upon the input/output power calculated for this device with optimized output loading. Note that neglecting the second harmonic significantly changes the output power in the saturation region. However, it is difficult to evaluate accurately the impedance seen at each harmonic in a given circuit. The impedance used for this calculation assumes lumped-element matching.

Fig. 15 shows the calculated load-pull contour for 175-mW output power for a second RCA device at 50-mW RF input power. However, in the experiment, the RF input

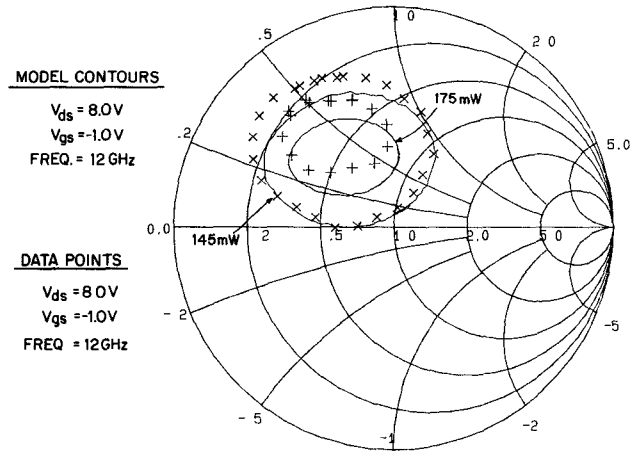


Fig. 12. Smith Chart display of calculated and measured load-pull contours for device B1512-3A at 12 GHz.

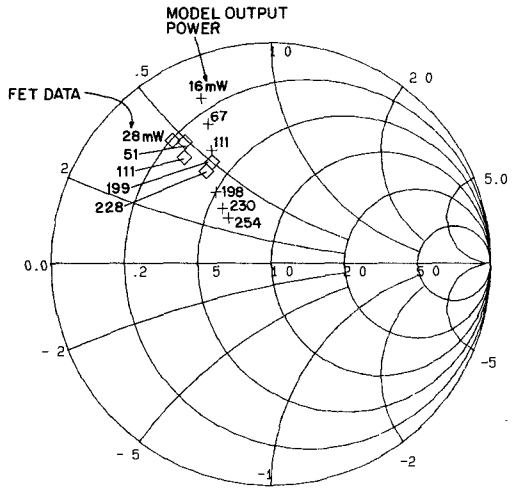


Fig. 13. Smith Chart display of calculated and measured optimum RF output loads for device B1512-3A at 12 GHz.

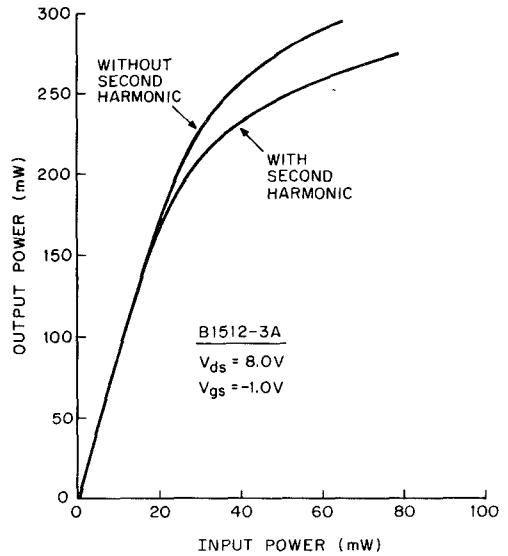


Fig. 14. RF output versus input calculated with and without second-harmonic voltages for device B1512-3A at 12 GHz.

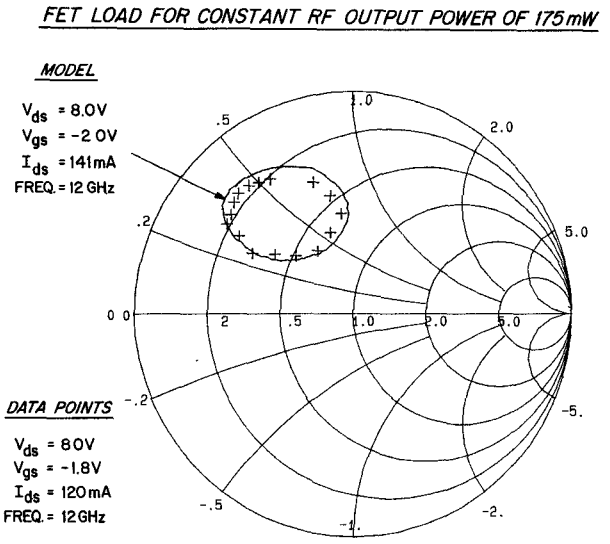


Fig. 15. Smith Chart display of calculated and measured RF output loads for constant output power of 175 mW for device B1824-1C at 12 GHz.

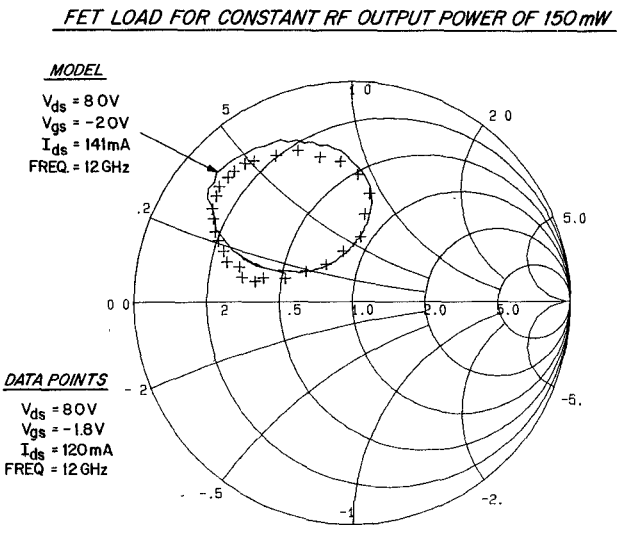


Fig. 16. Smith Chart display of calculated and measured RF output loads for constant output power of 150 mW for device B1824-1C at 12 GHz.

power was 104 mW. Fig. 16 shows the same comparison for an output power of 150 mW with the same drive conditions. There is good agreement with regard to output load-pull characteristics for a given output power, but disagreement in driver power (and gain) by approximately 3 dB. Some of this error is attributable to losses in the input tuner used in the measurements, although the actual value of tuner loss was not measured.

The maximum RF power output for the simulation with 50-mW input power is 216 mW. In the experiment using a 104-mW RF drive, the maximum RF power output was 205 mW.

Fig. 17 shows the load conditions for maximum power output at seven different output power values as computed by the nonlinear program. Measured data are also shown and are in good agreement.

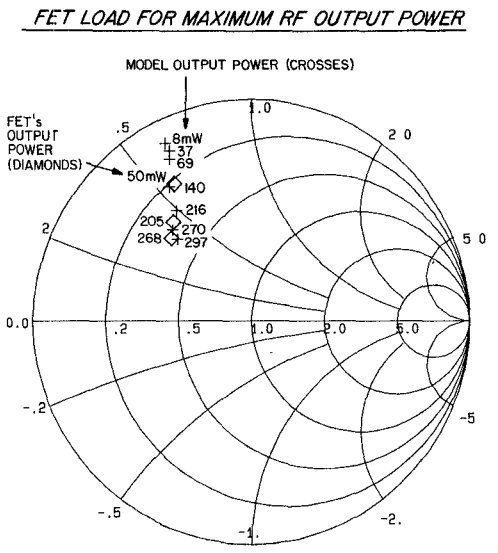


Fig. 17. Smith Chart display of calculated and measured optimum RF output loads for device B1824-1C at 12 GHz.

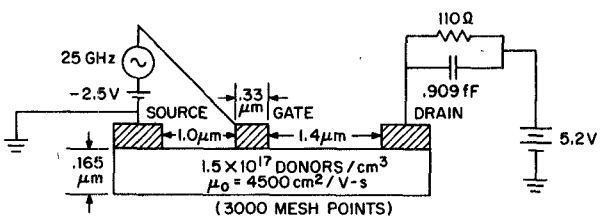


Fig. 18. Two-dimensional FET model parameters and the external circuits and voltage sources.

VII. Comparison of the Nonlinear Model with the Two-Dimensional FET Model

A direct comparison was made between the large-signal operation of the nonlinear FET model and that of an accurate two-dimensional (2-D) time-domain model for the GaAs FET. The 2-D model [17] includes carrier heating effects that produce velocity overshoot. In addition, the 2-D model produces voltage waveforms that are not restricted in harmonic content. Thus, it is possible to evaluate the accuracy of the nonlinear program with regard to the harmonic content of the voltage waveforms.

Fig. 18 shows the 2-D FET model and the external circuits and voltage sources. The gate is driven by a sinusoidal voltage source so negligible harmonic impedance will be assumed in the gate circuit for the nonlinear model. The drain load is 110 Ω shunted by a small capacitance to produce a time constant of 0.1 ps which is necessary to stabilize the solutions for the 2-D model. The FET is of short gate length (0.33 μm), high donor value ($1.5 \times 10^{17}/cm^3$), and 100-μm width. The average current under the bias voltage shown is 20.0 mA, which makes the average drain voltage approximately 3.0 V. The input RF frequency is 25 GHz.

Time-domain simulations were made using the 2-D model and circuit for RF input voltage amplitudes of 0.75, 1.5, and 2.5 V. Each required considerable computational time.

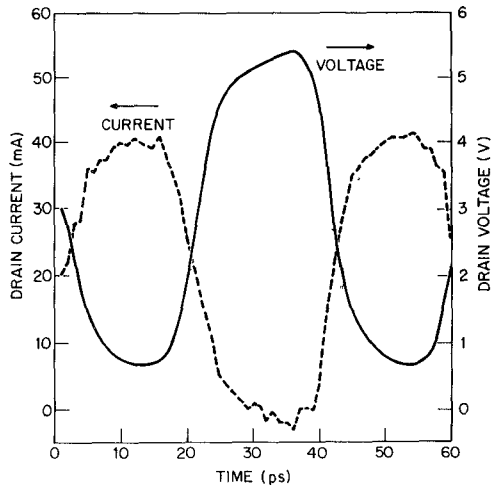


Fig. 19. Drain voltage and current waveforms for the two-dimensional FET simulation for gate-source ac amplitude of 2.5 V (Input power = 3.3 dBm).

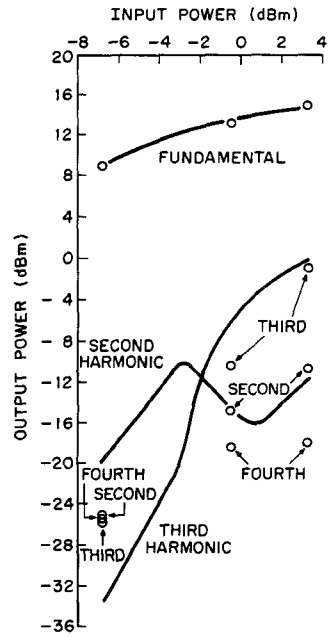


Fig. 20. Output power at fundamental-, second-, and third-harmonic frequencies as a function of input power. Solid lines are from NFET and points are from the two-dimensional model.

Fig 19 shows the drain voltage and current waveforms for an input amplitude of 2.5 V. The simulation was made for one and one-half RF cycles. The voltage waveform can be seen to be repeating indicating that it is a steady-state waveform. The current is not calculated as accurately and has computational fluctuations that are not physically meaningful. The voltage waveform was then Fourier analyzed to find its harmonic content for comparison with the nonlinear model.

The nonlinear FET model was developed in the following manner. A small-signal equivalent circuit model was evaluated for the 2-D FET operated at a drain-source bias of 3.0 V. The elements values are:

$$R_{\text{in}} = 6.04$$
$$C_{gs} = 0.0461 \text{ pF}$$
$$C_{dg} = 4.90 \text{ fF}$$
$$g_m = 17.50 \text{ mS}$$
$$\tau = 0.5 \text{ ps}$$
$$R_{ds} = 5280\ \Omega$$
$$C_{ds} = 0$$
$$R_s = 5.1$$
$$R_g = 0$$
$$R_d = 0$$
$$L_{\text{SOURCE}} = 0.$$

The 2-D model was also used to calculate the steady-state drain current as a function of gate-source and drain-source voltages. The coefficients for analytic approximation of $I_{ds}(V_{\text{in}}, V_{\text{out}})$ were then evaluated. Avalanche breakdown and gate forward biasing were neglected.

Using these device parameters, the nonlinear FET amplifier program was operated assuming the RF load shown in Fig. 18. The solid lines in Fig. 20 are values of harmonic power delivered to the load as calculated by the nonlinear program and the points are results of the 2-D simulations program.

The agreement is excellent for the fundamental output power. The agreement for second- and third-harmonic output power is good except at the lowest input power. Here the harmonic power calculation is clearly inaccurate in the 2-D program because all harmonic powers are the same, which is nonphysical. Only three harmonics are used in the nonlinear program so the fourth harmonic is not evaluated.

Notice particularly that the third-harmonic output power dominates in the FET. This effect has been observed experimentally by Willing *et al.* [11] and leads, we believe, to important third-order intermodulation distortion (IMD) in GaAs FET amplifiers. In fact, the IMD could be evaluated using the analytical model with some further programming effort.

Fig. 20 clearly shows that the nonlinear program accurately predicts saturation effects due to the nonlinear current control characteristic and also predicts harmonic power output accurately when harmonic impedances are accurately known. Once the parameters of the nonlinear model were known, it took 1/300 the computation time to generate the curves of Fig. 16 than it did to get the three cases with the 2-D model. The nonlinear model is clearly more efficient.

VIII. Conclusion

We have developed the FET model suitable for efficient calculation in the large-signal region. It is useful for developing optimized output network designs for high-power GaAs FET amplifiers. The program efficiency results from the use of the harmonic balance technique wherein the

nonlinear FET is analyzed in the time domain and the linear circuit is analyzed in the frequency domain.

The principle nonlinearities of the FET are voltage-controlled current sources. The nonlinearity of the reactive elements does not affect the large-signal solution greatly. However, it is necessary to evaluate the characteristics of the current sources for each device to be simulated. The simulation can be performed with a voltage waveform containing fundamental- and second-harmonic frequencies or fundamental-, second-, and third-harmonic frequencies. All FET current harmonics are included. The third harmonic is used only when accurate circuit impedance data is available at the third-harmonic frequency.

The nonlinear FET model was coupled to a program to generate constant output power contours on a Smith Chart. Excellent agreement was obtained with the measured load-pull characteristics at 12 GHz. However, the simulation predicted more gain than was measured in the experiments.

Finally, a comparison was made with large-signal simulations using an accurate 2-D model for the GaAs FET. This model includes carrier heating effects that produce the phenomenon of velocity overshoot. The output current and voltage waveforms in time could be directly compared for this case and the harmonic power contents were found to be in good agreement.

Appendix A
Dependence of the FET Parameters Upon Biasing

S-parameters were measured over a wide range of drain-source and gate-source voltages. The objective was to better understand the properties of the FET that contribute to good dc-to-RF power conversion. These measurements are useful because during large-signal operation, the device operating voltages have large excursion. Lumped-element circuit models were then constructed at each operating point.

The device tested (B1499-97) is capable of over 21-percent power-added efficiency at 20 GHz. Devices from this wafer have also operated at 35 GHz. This FET is representative of good but not the best of our devices.

Tables I and II show the values of the important equivalent circuit parameters as a function of gate-source voltage (Table I) and drain-source voltage (Table II). Although not presented here, we also have evaluated the circuit parameters at various gate-source voltages at $V_{ds}=1$, 2 and 4 V. The parameters in the table are

g_m	transconductance,
τ	current delay time,
C_{gs}	gate-source capacitance,
R_i	gate-source resistance,
C_{dg}	drain-gate capacitance,
R_{ds}	drain-source resistance.

The following conclusions can be drawn from these measurements.

1) R_{ds} is a strong function of V_{ds} and V_{gs} and is approximately proportional to V_{ds}.

2) g_m is a strong function of both V_{ds} and V_{gs}.

TABLE I
FET Equivalent Circuit Parameters as a Function of Gate-Source Bias for Device B1499-#97, $V_{ds}=8$ V

V_{gs} (V)	g_m (mS)	τ (ps)	C_{gs} (pF)	R_i (Ω)	C_{dg} (pF)	R_{ds} (Ω)
0	56.38	8.65	0.949	1.14	0.0141	515.2
-1	49.9	8.37	0.799	1.64	0.0200	422.9
-2	47.0	8.19	0.739	2.27	0.0259	326.2
-3	45.33	7.20	0.688	2.13	0.0327	269.1

TABLE II
FET Equivalent Circuit Parameters as a Function of Drain-Source Bias for Device B1499-#97, $V_{gs}=-2$ V

V_{ds} (V)	g_m (mS)	τ (ps)	C_{gs} (pF)	R_i (Ω)	C_{dg} (pF)	R_{ds} (Ω)
1	66.03	2.56	0.495	2.04	0.1993	22.4
2	63.97	3.11	0.607	1.82	0.0883	95.9
3	57.31	4.91	0.6614	1.65	0.050	171.3
8	47.00	8.19	0.739	2.27	0.0259	326.2

3) τ is a strong function of V_{ds} being approximately proportional to V_{ds}.

4) C_{dg} is a strong function of both V_{ds} and V_{gs}.

5) C_{gs} is a function of both V_{ds} and V_{gs}.

It is usually assumed that GaAs FET's follow a gate control characteristic resulting from a depletion depth calculable using a simple abrupt junction model. Neglecting source resistance, the saturated drain-source current I_{DS} is equal to

$$I_{DS}=I_p(1-d/a)$$

where

a	active layer thickness,
N_d	donor value,
Z	gate width,
v_s	saturated election drift velocity,
d	depletion depth,
V_{gs}	gate-source voltage,
V_{BI}	built-in voltage,
V_p	pinchoff voltage ($qN_da^2/2\epsilon$),

and

$$d/a=\left[(V_{BI}-V_{gs})/V_p\right]^{1/2}$$

$$I_p=qN_dZav_s.$$

By differentiation of I_{DS}, the intrinsic transconductance g_m is

$$g_m=\epsilon Zv_s/d.$$

The gate-source capacitance C_{gs} is approximately equal to

$$C_{gs}=\epsilon ZL_g/d$$

where L_g equals gate length. (Parasitic capacitances external to the conduction channel are not included in C_{gs}.) If

TABLE III
FET AVERAGE VELOCITY CALCULATION AS A FUNCTION OF DRAIN-SOURCE BIAS VOLTAGE FOR DEVICE B1499-#97, $V_{gs} = -2$ V

V_{ds} (V)	$\tau_{tt} = C_{gs}/g_m$ (ps)	$v_s = L_g/\tau_{tt}$ (10^7 cm/s)
1	7.50	1.33
2	9.48	1.05
4	11.54	0.867
8	15.72	0.636

TABLE IV
FET AVERAGE VELOCITY CALCULATIONS AS A FUNCTION OF GATE-SOURCE VOLTAGE FOR DEVICE B1499-#97, $V_{ds} = 8$ V

V_{gs} (V)	I_{ds} (mA)	$\tau_{tt} = C_{gs}/g_m$ (ps)	$v_s = L_g/\tau_{tt}$ (10^7 cm/s)
0	190	16.83	0.594
-1	125	16.01	0.625
-2	95	15.72	0.636
-3	75	15.18	0.659

the transit-time under gate τ_{tt} is defined as L_g/v_s, then

$$\tau_{tt} = L_g/v_s = C_{gs}/g_m.$$

Notice that there is no obvious dependence upon drain-source voltage although real devices show the following several dependencies.

1) C_{gs} increases strongly as V_{ds} increases. This indicates a reduction in the depletion layer depth d, probably due to increased lateral diffusion due to increased electron energy.

2) The transconductance g_m decreases as V_{ds} increases. Since d is decreasing, the saturated velocity v_s must be decreasing significantly as V_{ds} is increased.

3) C_{gs}/g_m increases strongly as V_{ds} increases. This is due to the decreasing v_s with V_{ds} increase.

4) The time-delay factor for transconductance τ changes little with V_{gs} but increases directly as V_{ds}. Since τ must be directly related to τ_{tt}, this effect is also a result of v_s dependency upon V_{ds}.

We will now quantitatively interpret the FET measurements. Table III lists the calculated values of τ_{tt} and v_s as a function of V_{ds}. Table III shows that there is a strong dependence upon V_{ds}. However, the biasing power varies greatly during variation of V_{ds} so it is important to verify that average heating effects are not responsible for the changes in v_s.

Table IV shows v_s as a function of V_{gs}. Here also there is a large change in bias power. However, there is negligible change in v_s in Table IV. Therefore average temperature effects are not important in the results of Table I. The strong dependence of average electron drift velocity on drain-source voltage clearly influences the FET frequency response.

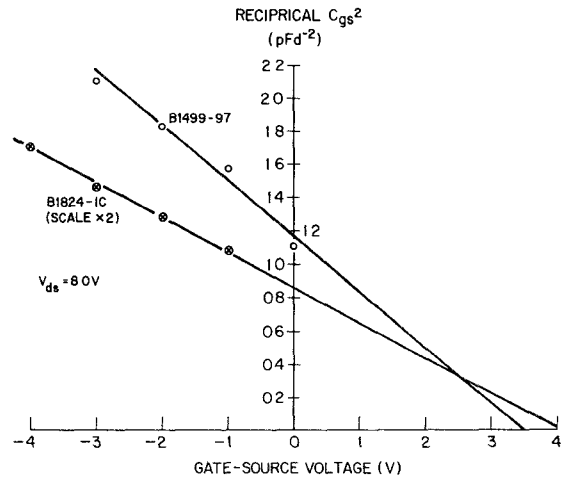


Fig. 21. Reciprical gate-source capacitance squared as a function of gate-source voltage as determined from small-signal models for two laboratory devices.

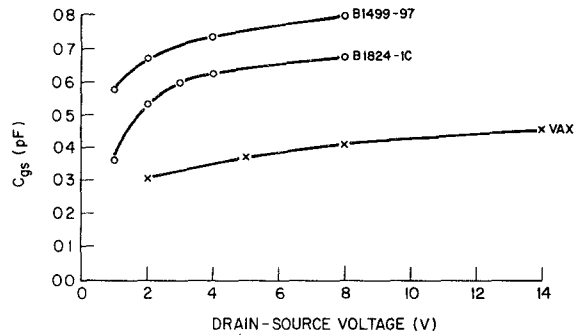


Fig. 22. Gate-source capacitance as a function of drain-source voltage as determined from small-signal measurements for two laboratory devices with $V_{gs} = -1$ V and for a two-dimensional simulation model with $V_{gs} = -2.75$ V.

APPENDIX B
GATE-SOURCE CAPACITANCE NONLINEARITY

The gate-source capacitance of a GaAs Schottky-barrier FET varies with both gate and drain voltage. However, measurements show that the variation is not large and it can often be neglected in nonlinear modeling.

Fig. 21 shows measured values of C_{gs}^{-2} plotted as a function of V_{gs}. The graphs are approximately linear as expected but the slopes are much less than expected. From the equations of Appendix A, it can be shown that, approximately

$$\frac{1}{C_{gs}^2} = \frac{2(V_{BI} - V_{gs})}{qNZ^2L_g^2}.$$

Separate measurements of the built-in voltage V_{BI} show it to be about 0.75 V. Since the above expression for C_{gs}^{-2} must go to zero value at $V_{gs} = V_{BI}$, we must conclude that there is significant fixed parasitic gate-source capacitance that is independent of the junction capacitance. This fixed capacitance reduces the percentage change in capacitance due to changes in V_{gs}.

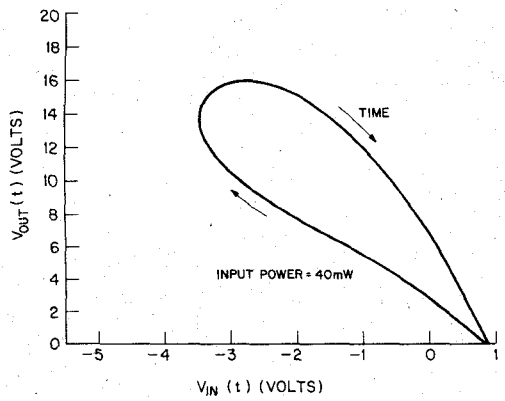


Fig. 23. Operating loci of input and output voltages for nonlinear simulations of FET B1512-3A with $V_{ds} = 8$ V, $V_{gs} = -1$ V, and output RF power = 154 mW.

Fig. 22 shows the variation in C_{gs} as a function of V_{ds} for two devices at $V_{gs} = -1$ V and for a 2-D model on the VAX 11/780 computer. All devices show an increase of C_{gs} with V_{ds}.

Clearly, C_{gs} increases with increase of V_{ds} and decrease of V_{gs}. However, in steady-state amplifier operation, V_{ds} is large when V_{gs} is small and vise-versa. Fig. 23 shows a typical relationship between V_{out} (or V_{ds}) and V_{in} (or V_{gs}) for large-signal operation of a typical device, as calculated by the nonlinear program. Based upon the measured data we assumed that

$$C_{gs} = 0.909\left[1 + 0.0125\, V_{\text{out}}(t)\right]\sqrt{\frac{3.75 - V_{gs}^{dc}}{3.75 - V_{\text{in}}(t)}} \cdot C_0$$

where C_0 is the value of C_{gs} at V_{gs}^{dc} and $V_{ds} = 8.0$ V. The variation for C_{gs} over the operating path of Fig. 23 as given by the above equation is less than 20 percent. This is the reason that nonlinear simulations that assume a fixed value of capacitance give very nearly the same solutions for RF power computations.

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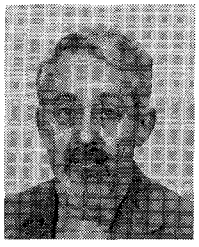

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